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Docket No.: 08211/0200388-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Vadim Tsinker

Patent No.: 6,850,181

Issued: February 1, 2005

For: APPARATUS AND METHOD FOR NOISE
REDUCTION FOR A SUCCESSIVE
APPROXIMATION ANALOG-TO-DIGITAL
CONVERTER CIRCUIT

Certificate
MAY 23 2005
of Correction

**REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322**

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted an error which should be corrected.

In the Specification:

First Page, Col. 2, Attorney, Agent, or Firm Delete "Mathew" and insert -- Matthew --.

Claim 1, Line 7, Column 11, Line 57, In Claim 1, after "the" insert -- first --.

Claim 2, Line 5, Column 12, Line 6, In Claim 2, after "from" delete "the".

Claim 13, Line 3, Line 12, In Claim 13, insert -- first -- before "second".


The error was not in the application as filed by applicant; accordingly no fee is required.

Enclosed please find copies of pages 18 & 20.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: May 11, 2005

Respectfully submitted,

By 
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The Commissioner is authorized to charge any deficiency or credit any excess in this fee to Deposit Account No. 04-0100.

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

Page 1 of 1

PATENT NO. : 6,850,181
APPLICATION NO. : 10/755,013
ISSUE DATE : February 1, 2005
INVENTOR(S) : Vadim Tsinker

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

First Page, Col. 2, Attorney, Agent, or Firm Delete "Mathew" and insert

-- Matthew --.

Claim 1, Line 7, Column 11, Line 57, In Claim 1, after "the" insert -- first --.

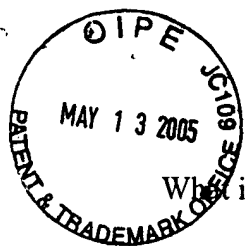
Claim 2, Line 5, Column 12, Line 6, In Claim 2, after "from" delete "the".

Claim 13, Line 3, Line 12, In Claim 13, insert -- first -- before "second".

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What is claimed is:

1. A circuit for successive approximation analog-to-digital conversion, comprising:
a noise-compensating comparator circuit that is configured to provide a
comparator output signal in response to a first comparison signal, a second comparison
signal, a first reference signal, and a second reference signal,

wherein the noise-compensating comparator circuit is configured to combine the
first comparison signal, the second comparison signal, the first reference signal, and the
first second reference signal to provide a differential signal such that a noise component
of the first comparison signal is substantially cancelled out;

a successive approximation logic circuit that is configured to provide a digital
output signal from the comparator output signal; and

a digital-to-analog converter circuit that is configured to provide the first
comparison signal from the digital output signal.

2. The circuit of Claim 1, wherein the noise-compensating comparator circuit is
configured to combine a signal derived from the first comparison signal with a signal
derived from the second reference signal to provide a first half of the differential signal,
and further configured to combine a signal derived from the second comparison signal
with a signal derived from first reference signal such that the noise component of the first
comparison signal is substantially cancelled out differentially.

3. The circuit of Claim 1, wherein the noise-compensating comparator circuit
includes:

a first differential pair, wherein the first differential pair includes a first transistor
and a second transistor;

a second differential pair, wherein the second differential pair having a third
transistor and a fourth transistor, a drain of the third transistor is coupled to a drain of the
second transistor, a drain of the fourth transistor is coupled to a drain of the first

9. The circuit of Claim 7, wherein the replicating circuit includes:
a plurality of capacitors; and
a plurality of switches, wherein the plurality of switches are coupled to the plurality of capacitors.
10. The circuit of Claim 9, wherein the digital-to-analog converter circuit includes a voltage divider configured to provide the first comparison signal according to a resistance ratio of the voltage divider, and
wherein the successive approximation logic circuit is configured to control the switching of the plurality of capacitors such that an impedance ratio of the plurality of capacitors is substantially similar to the resistance ratio of the voltage divider.
11. The circuit of Claim 9, wherein the plurality of capacitors is similar to capacitors of the digital-to-analog converter circuit, and wherein the plurality of switches is adapted to operate substantially similarly to how switches of the digital-to-analog converter circuit are adapted to operate.
12. The circuit of Claim 11, wherein the switches of the digital-to-analog converter are configured to open and close responsive to a number of bits of the digital output signal.
13. A method for successive approximation analog-to-digital conversion, comprising:
combining a first comparison signal, a second comparison signal, a first reference signal, and a first second reference signal to provide a differential signal;
comparing a first half and a second half of the differential signal to provide a comparison result signal;
employing successive approximation logic to provide a digital output signal from the comparison result signal; and
employing digital-to-analog conversion to provide the first comparison signal from the digital output signal.



Application No. (if known): 10/755,013

Attorney Docket No.: 08211/0200388-US0

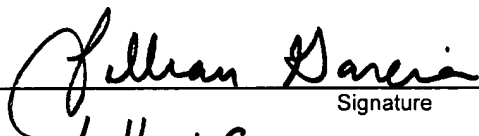
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on May 13, 2005
Date


Signature

Lillian Garcia

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Registration Number, if applicable

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Certificate of Correction (1 page)
Request for Certificate of Correction (2 pages)
Copy of Pages 18 & 20 of the claims (2 pages)
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